- Written and one-to-one oral communication skills
- Time management skills
- Knowledgeable and experience using VHDL to design complex circuits
- Experience designing circuits that interface with a bus and include a processor
- Previous experience synthesizing FPGA Designs that include processors
- Experience with the Xilinx Vivado tool flow
- Experience running software on bare metal
- Experience using software design tools (e.g. GDB)
- Experience writing device drivers
- Very knowledgeable of C/C++

The University is committed to the principle of equity in employment

The information submitted with your application is collected under the authority of the University Act (R.S.B.C. 1996, c.468, s. 27(4)(a)), applicable federal and provincial employment regulations and requirements, the University's non-academic employment policies and applicable collective agreements.

The information is related directly to and needed by the University to initiate the employment application process. The information will be used to contact references supplied by you, evaluate your qualifications and complete the employment process by making a hiring decision. Applicant information may also be disclosed to the Teaching Support Staff Union in accordance with Article XIII F.3.1.a (iv) of the Collective Agreement.

If you have any questions about the collection, use and disclosure of this information please contact the